WHAT IS CLAIMED IS:

1. A processing unit that handles processing of snoop related communications for a plurality of independent cache units of the processing unit based at least in part on whether the snoop related communications are initiated internally or externally with respect to the processing unit.

2. The processing unit of claim 1, wherein the processing unit handling processing of snoop related communications comprises the processing unit coordinating issuance of externally initiated snoops to maintain coherent snoop pipelines for the plurality of independent cache units.

3. The processing unit of claim 2, wherein coordinating issuance comprises the processing unit delaying issuance of an externally initiated snoop to the plurality of independent cache units at least until the plurality of independent cache units is capable of processing the externally initiated snoop.

4. The processing unit of claim 3, wherein the plurality of independent cache units is capable of processing the externally initiated snoop after completing processing of one or more previously issued snoops.

5. The processing unit of claim 3, wherein the processing unit issues internally initiated snoops without stalling.

6. The processing unit of claim 1, wherein the processing unit gathers from the plurality of independent cache units responses to externally initiated snoops and generates a snoop response for the processing unit based at least in part on the gathered independent cache units' snoop responses.

7. The processing unit of claim 6, wherein the processing unit supplies the generated processing unit response to a system bus.

8. The processing unit of claim 6, wherein the processing unit snoop response indicates a cache state based at least in part on caches states of respective cache unit caches.

9. The processing unit of claim 6, wherein the processing unit response is further based at least in part on one or more of bus states and cycle states.

10. The processing unit of claim 1, wherein each of the plurality of cache units includes one or more of instruction cache, data cache, L2 cache, and L3 cache.

11. A method of operating a multi-cache processing unit in a system with multiple processing units, the method comprising:

issuing to multiple cache units of the processing unit, snoops initiated externally with respect to the processing unit; and

supplying a unified response to the system from the processing unit, wherein the unified response is based at least in part on combination of cache responses to externally initiated snoops.

12. The method of claim 11, further comprising storing snoop addresses in respective queues of the cache.

13. The method of claim 12, further comprising delaying issuance of the snoop addresses that correspond to an externally initiated snoop at least until the cache units have completed prior pending snoop processing.

14. The method of claim 12, further comprising indicating initiators of externally initiated snoops in a common store for the cache.

15. The method of claim 11, wherein the unified response indicates a cache state for the processing unit that is based at least in part on states of the multiple cache.

16. The method of claim 15, wherein snoop responses are in accordance with a cache coherency protocol that includes one or more of a MOESI cache coherency

protocol, a MESI cache coherency protocol, a MOSI cache coherency protocol, and a MSI cache coherency protocol.

17. The method of claim 23, wherein the unified response indicates miss if cache responses indicate miss, clean if at least one of the cache responses indicate clean, shared if at least one of the cache responses indicate shared, or dirty if at least one of the cache responses indicate dirty.

18. The method of claim 11 further comprising supplying an internal snoop response to the initiating cache unit.

19. The method of claim 11 further comprising generating a unified internal snoop response based at least in part on cache responses to an internally initiated snoop and supplying the unified internal snoop response to the initiating cache unit.

20. The method of claim 11 embodied as a computer program product encoded in one or more machine-readable media.

21. A method comprising:

determining if a snoop is externally initiated or internally initiated with respect to a domain;

if the snoop is internally initiated,

issuing the snoop from the internal first cache unit that initiates the snoop to an internal second cache unit, wherein the first and second cache units are of the domain,

supplying an internal snoop response from the second cache unit to the first cache unit; and

if the snoop is externally initiated,

issuing the externally initiated snoop to the first and second cache units,

generating a processing unit response based at least in part on responses from the first and second cache units, and

supplying the processing unit response at least to the source of the externally initiated snoop.

22. The method of claim 21, further comprising:

if the snoop is externally initiated,

indicating the source of the snoop in a first encoding;

indicating the snoop address in snoop queue for the first cache unit and in a snoop queue for the second cache unit; and

storing the first supplied cache response from the cache units at least until the second cache response is supplied.

23. The method of claim 21, wherein snoop responses are in accordance with a cache coherency protocol that includes one or more of a MOESI cache coherency protocol, a MESI cache coherency protocol, a MOSI cache coherency protocol, and a MSI cache coherency protocol.

24. The method of claim 23, wherein the generated processing unit response indicates miss if both cache responses indicate miss, shared if at least one of the cache responses indicate shared, clean if at least one of the cache responses indicate clean, or dirty if at least one of the cache responses indicate dirty.

25. The method of claim 21 further comprising delaying issuance of the externally initiated snoop at least until the first and second cache units have completed processing of one or more prior pending snoops.

26. The method of claim 21 further comprising:

issuing the internally initiated snoop to a third internal cache unit;

supplying the internal response to the first internal cache unit, wherein the internal response is based at least in part on the second cache unit's response and the third cache unit's response.

27. The method of claim 21 further comprising delaying issuance of the snoop if the snoop address overlaps an address of an internal cache miss of a read or write operation at least until arrival of data for the internal cache miss.

28. The method of claim 21, wherein the domain corresponds to one or more of a processing unit of a multi-processing unit system and a port.

29. The method of claim 28 wherein the port includes a JBus port.

30. The method of claim 21 embodied as a computer program product encoded in one or more machine-readable media.

31. An integrated circuit comprising:

a plurality of cache units, each of the plurality of cache units having at least one cache;

a snoop controller for the integrated circuit, the snoop controller coupled with the plurality of cache units and the snoop controller having,

a snoop information store having a plurality of entries, each of the entries to indicate source of a snoop and whether a snoop is being processed;

snoop address stores to indicate addresses of corresponding snoops indicated in the snoop information store, wherein the snoop address stores indicate addresses for respective ones of the plurality of cache units; and

a snoop control logic coupled with the snoop information store and the snoop address stores, the snoop control logic to issue an externally initiated snoop to the plurality of cache units and to combine cache unit snoop responses to an externally initiated snoop.

32. The integrated circuit of claim 31, wherein indication of snoop source includes one or more of source identifier and whether a snoop is internally initiated or externally initiated.

33. The integrated circuit of claim 31, wherein the snoop address stores and the snoop information store include first-in-first-out queues.

34. The integrated circuit of claim 33, wherein the snoop control logic maintains read and write pointers for the snoop information store and the snoop address stores.

35. The integrated circuit of claim 31 further comprising an internal cache miss store to record internal cache misses of read and write operations, wherein the snoop control logic prevents issuance of snoops with target addresses that overlap addresses indicated in the local miss store, at least until indication that data of the cache misses has arrived.

36. The integrated circuit of claim 35, wherein the local miss store includes one or more of summing content addressable memory and content addressable memory.

37. The integrated circuit of claim 31 further comprising a response store to host snoop responses at least until gathered.

38. The integrated circuit of claim 37 further comprising the snoop controller logic to gather a first cache unit snoop response from the response store with a second cache unit snoop response, and to generate a unified snoop response based at least in part on the first and second cache unit snoop responses.

39. The apparatus of claim 37, wherein the response store includes entries sufficient to store responses from at most less than all of the plurality of cache units.

40. The integrated circuit of claim 31, wherein the cache includes one or more of L1 cache, L2 cache, and L3 cache.

41. An apparatus comprising:

a plurality of cache units; and

a snoop controller to determine whether snoops are initiated externally or internally with respect to the plurality of cache units and to issue snoops in accordance with the determination.

42. The apparatus of claim 41 further comprising the snoop controller to coordinate issuance of an externally initiated snoop to the plurality of cache units.

43. The apparatus of claim 42, wherein the snoop controller to coordinate issuance comprises the snoop controller to delay issuance of an externally initiated snoop at least until the plurality of cache units are capable of processing the externally initiated snoop.

44. The apparatus of claim 43, wherein the snoop controller delays issuance of externally initiated snoops to ensure cache unit snoop pipelines conform to sequential snoop constraints.

45. The apparatus of claim 41 further comprising the snoop controller to issue internally initiated snoops without delay.

46. The apparatus of claim 41 further comprising the snoop controller to coherently gather cache responses to an externally initiated snoop.

47. The apparatus of claim 46, wherein the snoop controller to coherently gather cache responses to the externally initiated snoop comprises the snoop controller to generate a unified snoop response based at least in part on the gathered cache responses.

48. The apparatus of claim 41 further comprising a bus arbiter to arbitrate between internal events and bus events.

49. The apparatus of claim 48, wherein the bus arbiter gives priority to bus events over internal events.

50. The apparatus of claim 41 further comprising an internal cache miss store to record addresses of internal cache misses of one or more read and write operations.

51. The apparatus of claim 50, further comprising the snoop controller to compare snoops against contents of the internal cache miss store, and to prevent issuance of snoops with addresses that overlap with addresses recorded in the internal cache miss store.

52. The apparatus of claim 51 further comprising a content addressable memory used by the snoop controller to compare snoop addresses with addresses recorded in the internal cache miss store.

53. An apparatus comprising:

a plurality of cache units; and

means for determining source of a snoop and for issuing the snoop in accordance with the determination, wherein the snoop is issued to the plurality of cache units if the snoop is determined to be externally initiated.

54. The apparatus of claim 53 further comprising means for blocking snoops with target addresses that overlap target addresses of internal cache misses at least until indication of data arrival.

55. The apparatus of claim 53 further comprising a bus arbiter to arbitrate internal events and bus events, wherein the bus arbiter handles bus events with priority over internal events.

56. The apparatus of claim 53 further comprising means to merge cache responses to externally initiated snoop.

57. A system comprising:

a system bus; and

a plurality of processing units, wherein at least one of the processing units include a plurality of cache units, the multi-cache unit processing unit having a snoop controller to determine whether snoops are initiated externally or internally and to issue snoops to the plurality of cache units in accordance with the determination.

58. The system of claim 57, wherein the multi-cache unit processor has a port to communicate snoop responses from the plurality of cache units.

59. The system of claim 58, wherein the multi-cache unit processor supplies unified snoop responses to the system, wherein the unified snoop responses are based at least in part on cache unit snoop responses.

60. The system of claim 58, wherein the port includes a JBus port.

61. The system of claim 57 wherein the snoop controller delays issuance of an externally initiated snoop to the plurality of cache units at least until the plurality of cache units are capable of processing the externally initiated snoop.

62. The system of claim 57, wherein the snoop controller issues internally initiated snoops without delay.